LM555 Timer

1 Features

- Direct Replacement for SE555/NE555
- Timing from Microseconds through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- Output Can Source or Sink 200 mA
- Output and Supply TTL Compatible
- Temperature Stability Better than 0.005% per °C
- Normally On and Normally Off Output
- Available in 8-pin VSSOP Package

2 Applications

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Linear Ramp Generator

3 Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM555	SOIC (8)	4.90 mm × 3.91 mm
	PDIP (8)	9.81 mm × 6.35 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Schematic Diagram

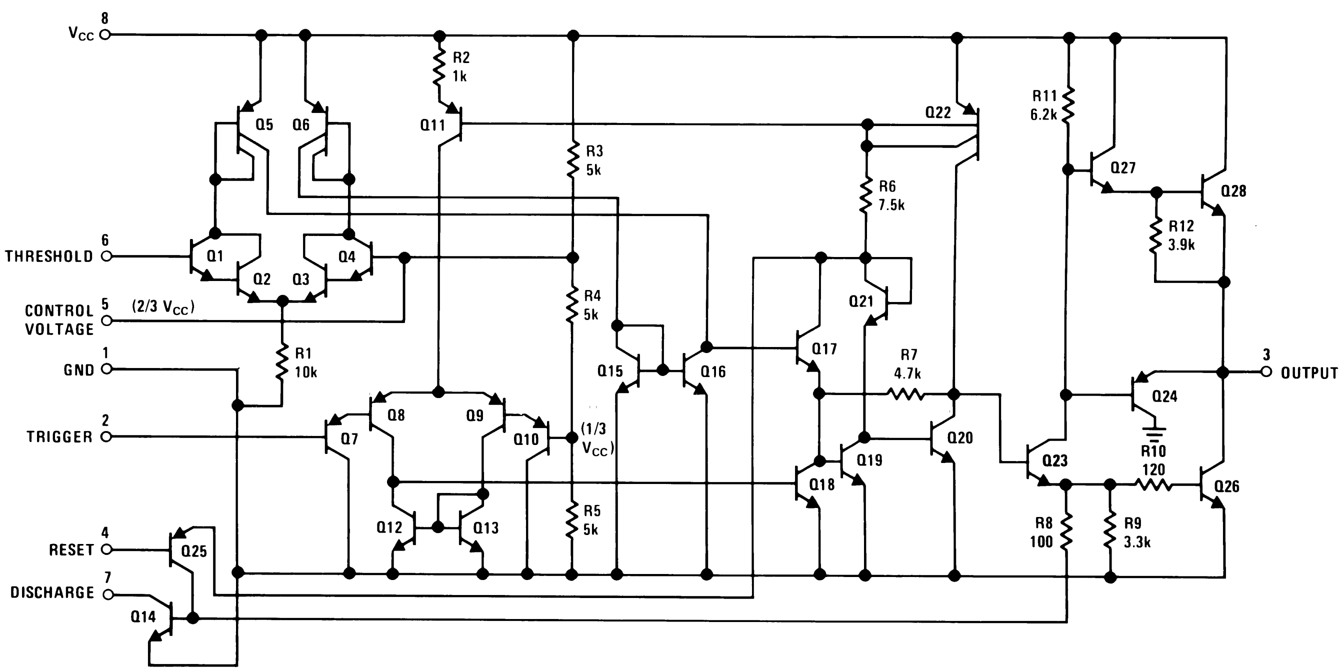


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4 Revision History

Changes from Revision C (March 2013) to Revision D — **Page**

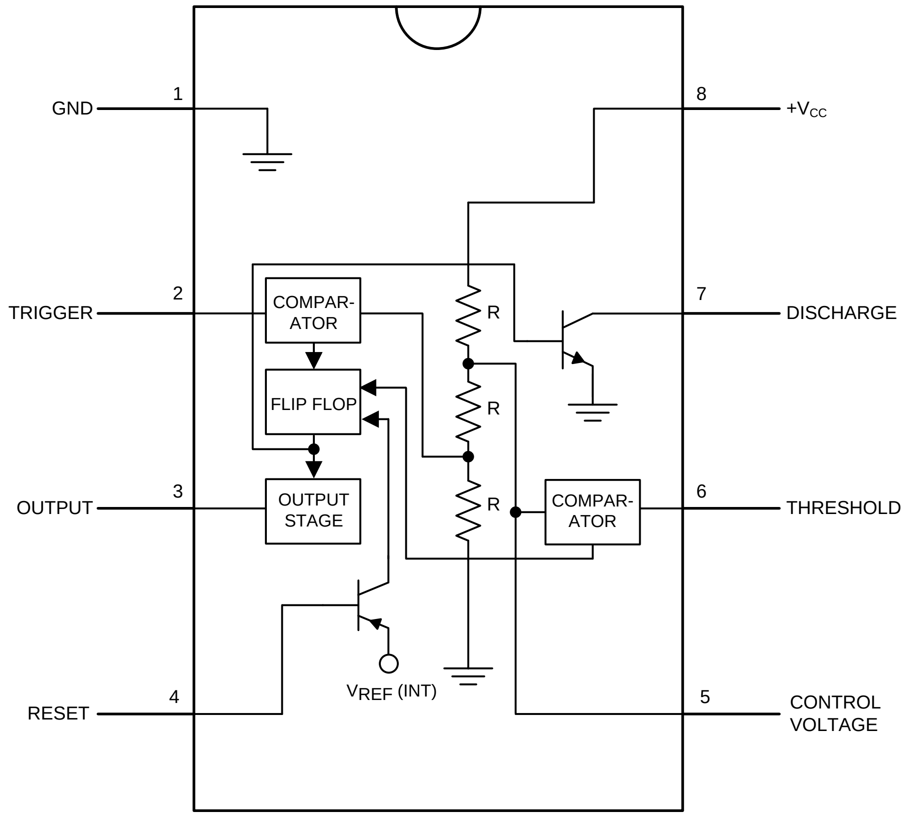
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision B (March 2013) to Revision C — **Page**

- Changed layout of National Data Sheet to TI format 13

5 Pin Configuration and Functions

D, P, and DGK Packages
8-Pin PDIP, SOIC, and VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
5	Control Voltage	I	Controls the threshold and trigger levels. It determines the pulse width of the output waveform. An external voltage applied to this pin can also be used to modulate the output waveform
7	Discharge	I	Open collector output which discharges a capacitor between intervals (in phase with output). It toggles the output from high to low when voltage reaches 2/3 of the supply voltage
1	GND	O	Ground reference voltage
3	Output	O	Output driven waveform
4	Reset	I	Negative pulse applied to this pin to disable or reset the timer. When not used for reset purposes, it should be connected to VCC to avoid false triggering
6	Threshold	I	Compares the voltage applied to the terminal with a reference voltage of 2/3 Vcc. The amplitude of voltage applied to this terminal is responsible for the set state of the flip-flop
2	Trigger	I	Responsible for transition of the flip-flop from set to reset. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin
8	V^+	I	Supply voltage with respect to GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
Power Dissipation(3)		LM555CM, LM555CN(4)		1180	mW
		LM555CMM		613	mW
Soldering Information	PDIP Package	Soldering (10 Seconds)		260	°C
	Small Outline Packages (SOIC and VSSOP)	Vapor Phase (60 Seconds)		215	°C
		Infrared (15 Seconds)		220	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) For operating at elevated temperatures the device must be derated above 25°C based on a 150°C maximum junction temperature and a thermal resistance of 106°C/W (PDIP), 170°C/W (S0IC-8), and 204°C/W (VSSOP) junction to ambient.
(4) Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500(2)	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The ESD information listed is for the SOIC package.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage		18	V
Temperature, T_A	0	70	°C
Operating junction temperature, T_J		70	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM555			UNIT
		PDIP	SOIC	VSSOP	
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106	170	204	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

(T_A = 25°C, V_{CC} = 5 V to 15 V, unless otherwise specified)[(1)(2)]

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage		4.5		16	V
Supply Current	V_{CC} = 5 V, R_L = ∞		3	6	mA
	V_{CC} = 15 V, R_L = ∞ (Low State) [(3)]		10	15	
Timing Error, Monostable					
Initial Accuracy			1 %		
Drift with Temperature	R_A = 1 k to 100 kΩ,		50		ppm/°C
	C = 0.1 μF, [(4)]				
Accuracy over Temperature			1.5 %		
Drift with Supply			0.1 %		V
Timing Error, Astable					
Initial Accuracy			2.25		
Drift with Temperature	R_A, R_B =1 k to 100 kΩ,		150		ppm/°C
	C = 0.1 μF, [(4)]				
Accuracy over Temperature			3.0%		
Drift with Supply			0.30 %		/V
Threshold Voltage			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15 V		5		V
	V_{CC} = 5 V		1.67		V
Trigger Current			0.5	0.9	μA
Reset Voltage		0.4	0.5	1	V
Reset Current			0.1	0.4	mA
Threshold Current	[(5)]		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15 V	9	10	11	V
	V_{CC} = 5 V	2.6	3.33	4	
Pin 7 Leakage Output High			1	100	nA
Pin 7 Sat [(6)]					
Output Low	V_{CC} = 15 V, I_7 = 15 mA		180		mV
Output Low	V_{CC} = 4.5 V, I_7 = 4.5 mA		80	200	mV
Output Voltage Drop (Low)	V_{CC} = 15 V				
	I_{SINK} = 10 mA		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.5	V
	I_{SINK} = 200 mA		2.5		V
	V_{CC} = 5 V				
	I_{SINK} = 8 mA				V
	I_{SINK} = 5 mA		0.25	0.35	V

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is functional, but do not ensure specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which ensures specific performance limits. This assumes that the device is within the *Recommended Operating Conditions*. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Supply current when output high typically 1 mA less at V_{CC} = 5 V.
(4) Tested at V_{CC} = 5 V and V_{CC} = 15 V.
(5) This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total ($R_A + R_B$) is 20 MΩ.
(6) No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Electrical Characteristics (continued)

(T_A = 25°C, V_{CC} = 5 V to 15 V, unless otherwise specified)(1)(2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15 V		12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15 V	12.75	13.3		V
	V_{CC} = 5 V	2.75	3.3		V
Rise Time of Output			100		ns
Fall Time of Output			100		ns

6.6 Typical Characteristics

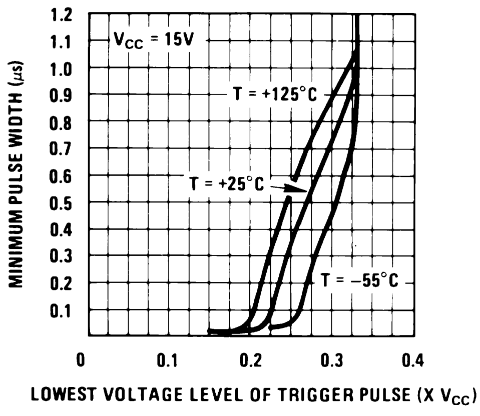


Figure 1. Minimum Pulse Width Required For Triggering

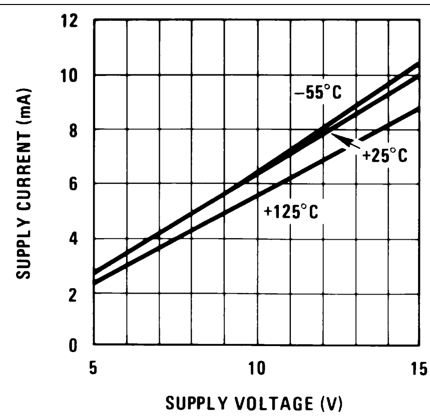


Figure 2. Supply Current vs. Supply Voltage

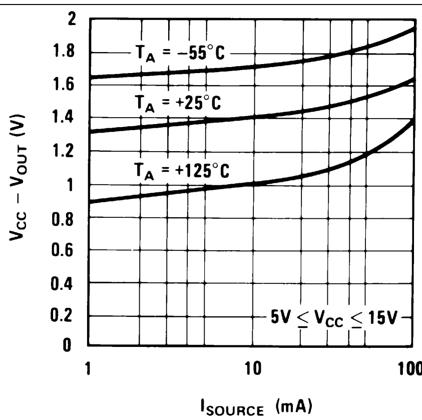


Figure 3. High Output Voltage vs. Output Source Current

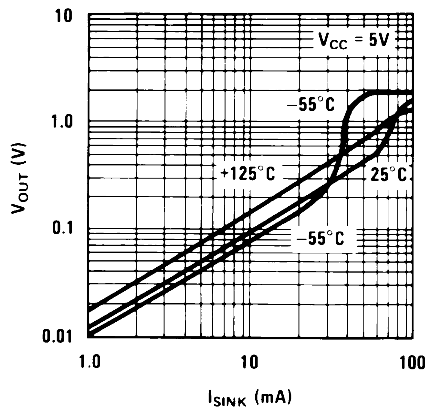


Figure 4. Low Output Voltage vs. Output Sink Current

Typical Characteristics (continued)

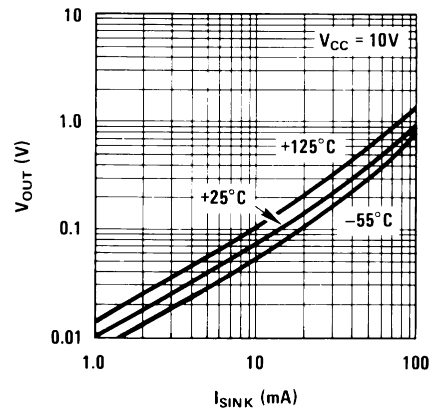


Figure 5. Low Output Voltage vs. Output Sink Current

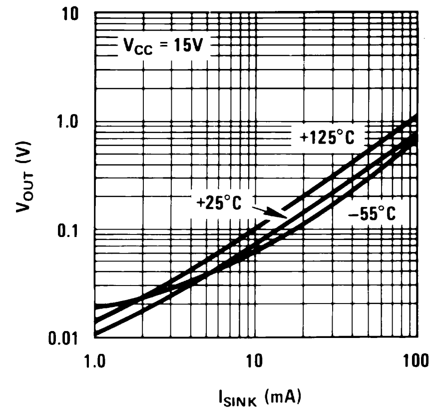


Figure 6. Low Output Voltage vs. Output Sink Current

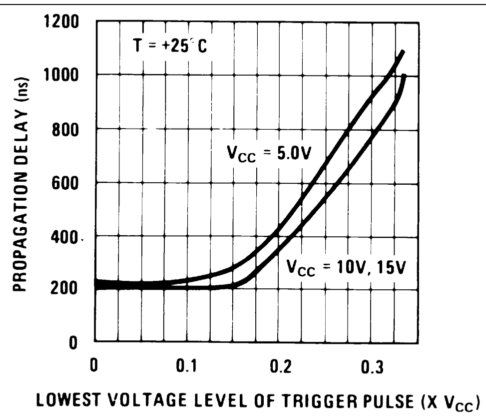


Figure 7. Output Propagation Delay vs. Voltage Level of Trigger Pulse

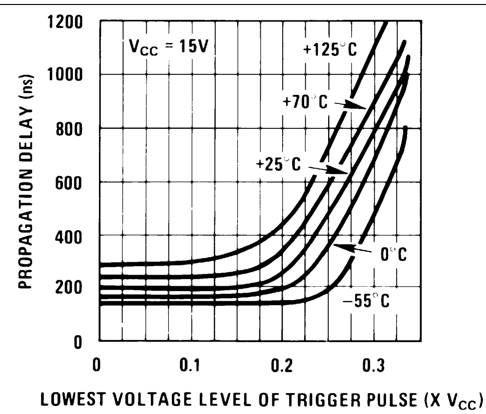


Figure 8. Output Propagation Delay vs. Voltage Level of Trigger Pulse

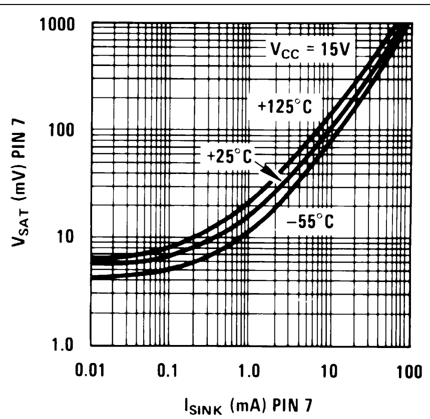


Figure 9. Discharge Transistor (Pin 7) Voltage vs. Sink Current

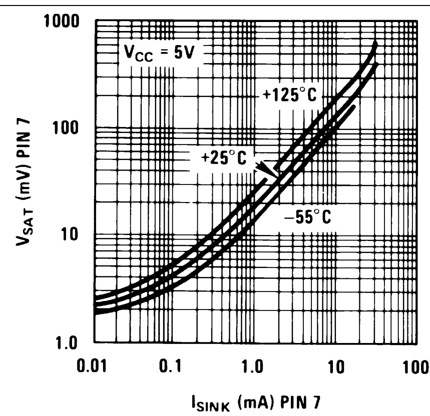


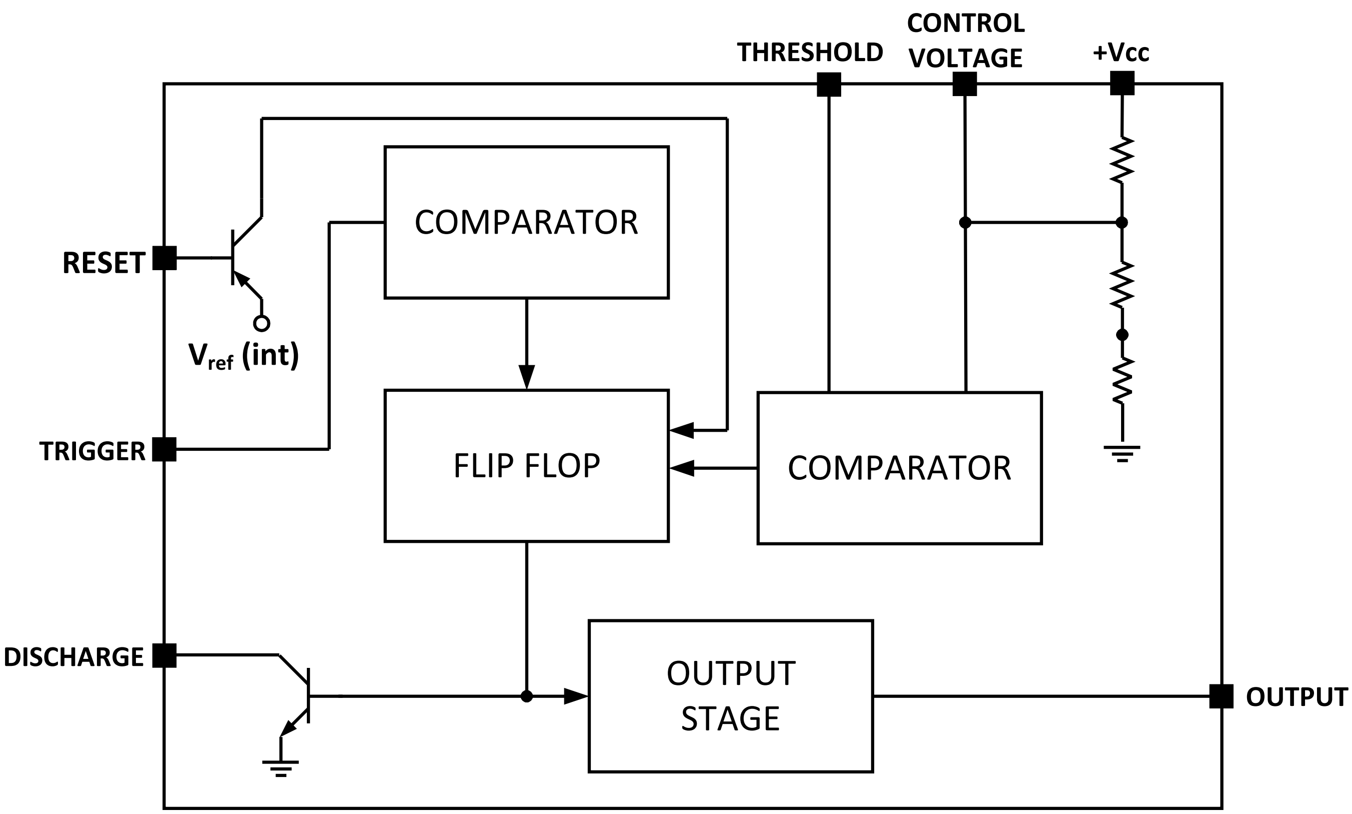
Figure 10. Discharge Transistor (Pin 7) Voltage vs. Sink Current

7 Detailed Description

7.1 Overview

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or driver TTL circuits. The LM555 are available in 8-pin PDIP, SOIC, and VSSOP packages and is a direct replacement for SE555/NE555.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Direct Replacement for SE555/NE555

The LM555 timer is a direct replacement for SE555 and NE555. It is pin-to-pin compatible so that no schematic or layout changes are necessary. The LM555 come in an 8-pin PDIP, SOIC, and VSSOP package.

7.3.2 Timing From Microseconds Through Hours

The LM555 has the ability to have timing parameters from the microseconds range to hours. The time delay of the system can be determined by the time constant of the R and C value used for either the monostable or astable configuration. A nomograph is available for easy determination of R and C values for various time delays.

7.3.3 Operates in Both Astable and Monostable Mode

The LM555 can operate in both astable and monostable mode depending on the application requirements.

- Monostable mode: The LM555 timer acts as a “one-shot” pulse generator. The pulse beings when the LM555 timer receives a signal at the trigger input that falls below a 1/3 of the voltage supply. The width of the output pulse is determined by the time constant of an RC network. The output pulse ends when the voltage on the

Feature Description (continued)

capacitor equals 2/3 of the supply voltage. The output pulse width can be extended or shortened depending on the application by adjusting the R and C values.

- Astable (free-running) mode: The LM555 timer can operate as an oscillator and puts out a continuous stream of rectangular pulses having a specified frequency. The frequency of the pulse stream depends on the values of R_A, R_B, and C.

7.4 Device Functional Modes

7.4.1 Monostable Operation

In this mode of operation, the timer functions as a one-shot (Figure 11). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

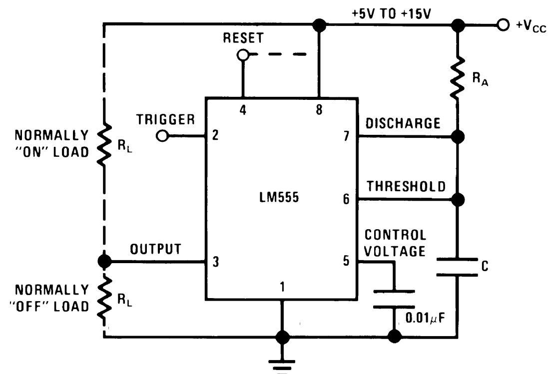
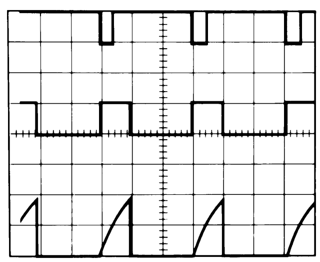


Figure 11. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_A C, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. Figure 12 shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.



V_{CC} = 5 V — Top Trace: Input 5V/Div.
TIME = 0.1 ms/DIV. — Middle Trace: Output 5V/Div.
R_A = 9.1 kΩ — Bottom Trace: Capacitor Voltage 2V/Div.
C = 0.01 μF

Figure 12. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10 μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, TI recommends connecting the Reset pin to V_{CC} to avoid any possibility of false triggering.

Device Functional Modes (continued)

Figure 13 is a nomograph for easy determination of R, C values for various time delays.

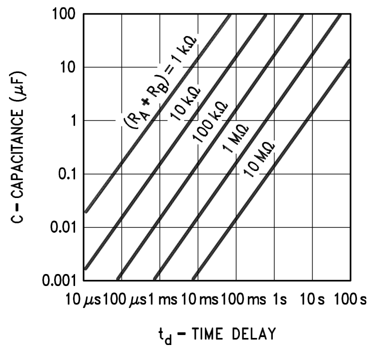


Figure 13. Time Delay

7.4.2 Astable Operation

If the circuit is connected as shown in Figure 14 (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

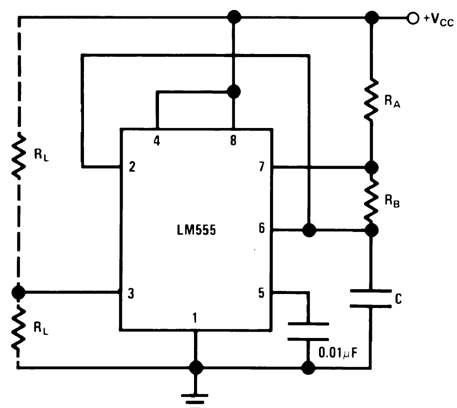
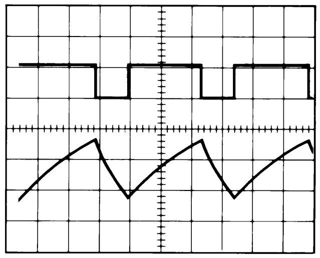


Figure 14. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 15 shows the waveforms generated in this mode of operation.

Device Functional Modes (continued)



V_{CC} = 5 V
TIME = 20μs/DIV.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 μF

Top Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

Figure 15. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C \tag{1}$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C \tag{2}$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C \tag{3}$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2\,R_B)\,C} \tag{4}$$

Figure 16 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B} \tag{5}$$

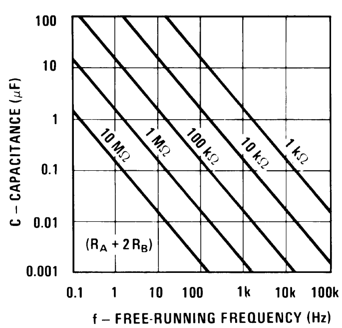


Figure 16. Free Running Frequency

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM555 timer can be used a various configurations, but the most commonly used configuration is in monostable mode. A typical application for the LM555 timer in monostable mode is to turn on an LED for a specific time duration. A pushbutton is used as the trigger to output a high pulse when trigger pin is pulsed low. This simple application can be modified to fit any application requirement.

8.2 Typical Application

Figure 17 shows the schematic of the LM555 that flashes an LED in monostable mode.

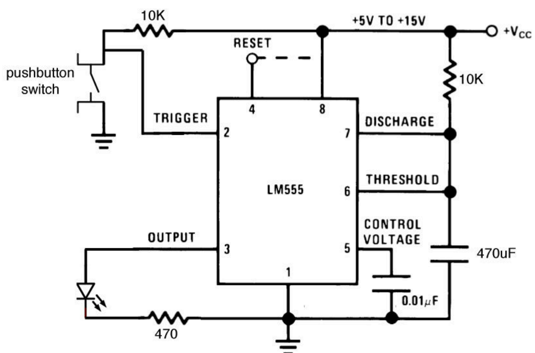


Figure 17. Schematic of Monostable Mode to Flash an LED

8.2.1 Design Requirements

The main design requirement for this application requires calculating the duration of time for which the output stays high. The duration of time is dependent on the R and C values (as shown in Figure 17) and can be calculated by:

$$t = 1.1 \times R \times C \text{ seconds} \quad (6)$$

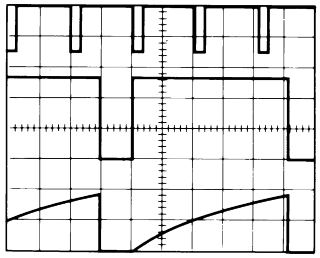
8.2.2 Detailed Design Procedure

To allow the LED to flash on for a noticeable amount of time, a 5 second time delay was chosen for this application. By using Equation 6, RC equals 4.545. If R is selected as 100 kΩ, C = 45.4 µF. The values of R = 100 kΩ and C = 47 µF was selected based on standard values of resistors and capacitors. A momentary push button switch connected to ground is connected to the trigger input with a 10-K current limiting resistor pullup to the supply voltage. When the push button is pressed, the trigger pin goes to GND. An LED is connected to the output pin with a current limiting resistor in series from the output of the LM555 to GND. The reset pin is not used and was connected to the supply voltage.

8.2.2.1 Frequency Divider

The monostable circuit of Figure 11 can be used as a frequency divider by adjusting the length of the timing cycle. Figure 18 shows the waveforms generated in a divide by three circuit.

Typical Application (continued)



V_{CC} = 5 V
TIME = 20 μs/DIV.
R_A = 9.1 kΩ
C = 0.01 μF

Top Trace: Input 4 V/Div.
Middle Trace: Output 2V/Div.
Bottom Trace: Capa citor 2V/Div.

Figure 18. Frequency Divider

8.2.2.2 Additional Information

Lower comparator storage time can be as long as 10 μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10 μs minimum.

Delay time reset to output is 0.47 μs typical. Minimum reset pulse width must be 0.3 μs, typical.

Pin 7 current switches within 30 ns of the output (pin 3) voltage.

8.2.3 Application Curves

The data shown below was collected with the circuit used in the typical applications section. The LM555 was configured in the monostable mode with a time delay of 5.17 s. The waveforms correspond to:

- Top Waveform (Yellow) – Capacitor voltage
- Middle Waveform (Green) – Trigger
- Bottom Waveform (Purple) – Output

As the trigger pin pulses low, the capacitor voltage starts charging and the output goes high. The output goes low as soon as the capacitor voltage reaches 2/3 of the supply voltage, which is the time delay set by the R and C value. For this example, the time delay is 5.17 s.

Typical Application (continued)

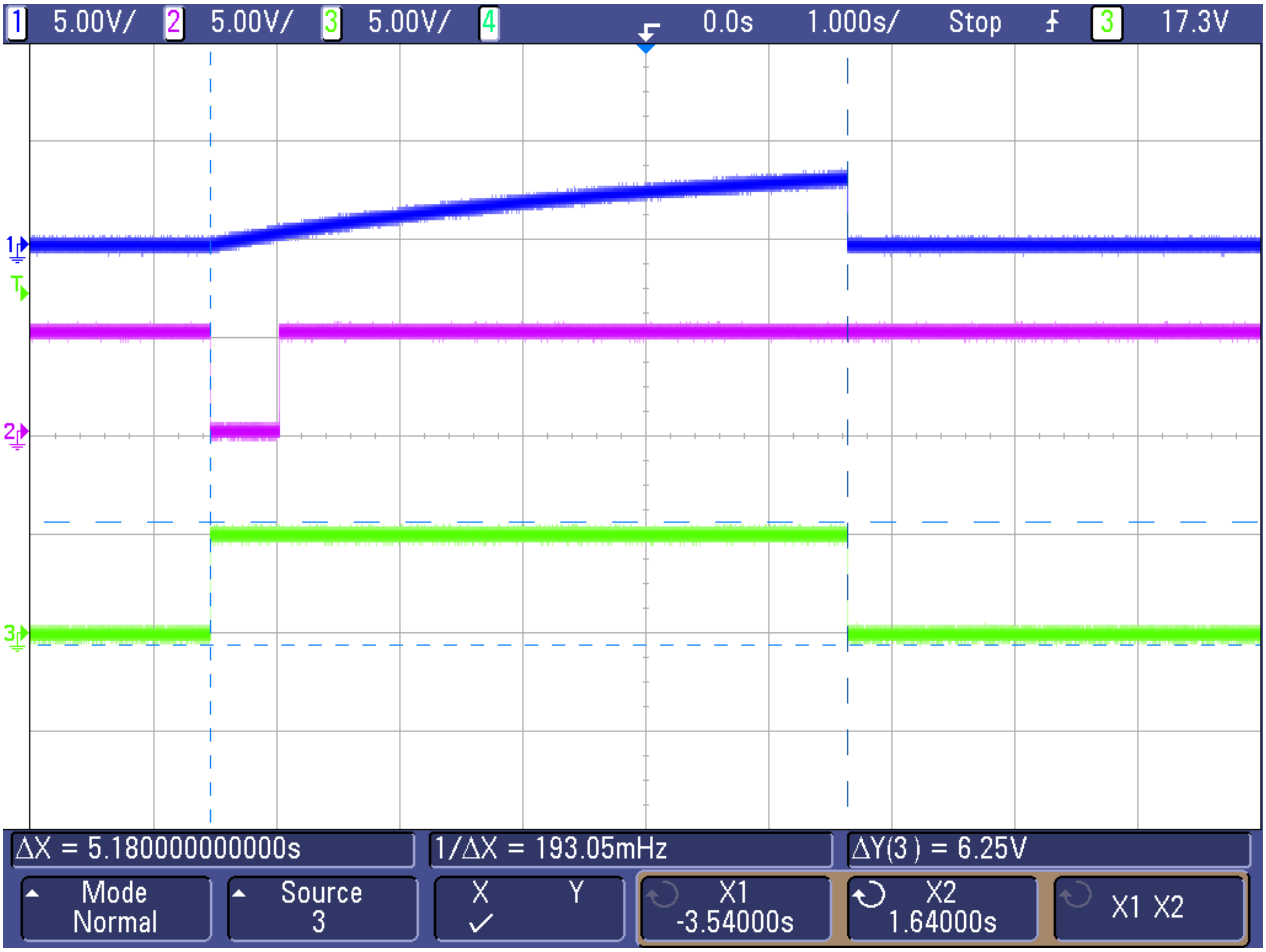


Figure 19. Trigger, Capacitor Voltage, and Output Waveforms in Monostable Mode

9 Power Supply Recommendations

The LM555 requires a voltage supply within 4.5 V to 16 V. Adequate power supply bypassing is necessary to protect associated circuitry. The minimum recommended capacitor value is 0.1 μF in parallel with a 1-μF electrolytic capacitor. Place the bypass capacitors as close as possible to the LM555 and minimize the trace length.

10 Layout

10.1 Layout Guidelines

Standard PCB rules apply to routing the LM555. The 0.1-μF capacitor in parallel with a 1-μF electrolytic capacitor should be as close as possible to the LM555. The capacitor used for the time delay should also be placed as close to the discharge pin. A ground plane on the bottom layer can be used to provide better noise immunity and signal integrity.

Figure 20 is the basic layout for various applications.

- C1 – based on time delay calculations
- C2 – 0.01-μF bypass capacitor for control voltage pin
- C3 – 0.1-μF bypass ceramic capacitor
- C4 – 1-μF electrolytic bypass capacitor
- R1 – based on time delay calculations
- U1 – LMC555

10.2 Layout Example

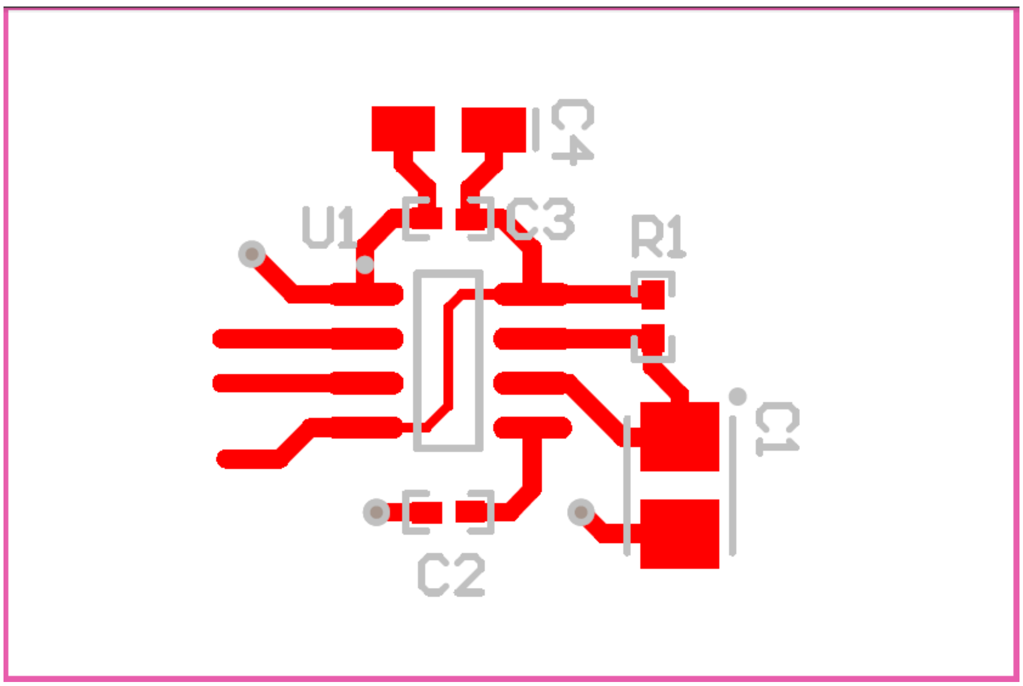


Figure 20. Layout Example

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM555CM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	LM 555CM	
LM555CM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM 555CM	Samples
LM555CMM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	0 to 70	Z55	
LM555CMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	Z55	Samples
LM555CMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	Z55	Samples
LM555CMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	LM 555CM	
LM555CMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM 555CM	Samples
LM555CN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LM 555CN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

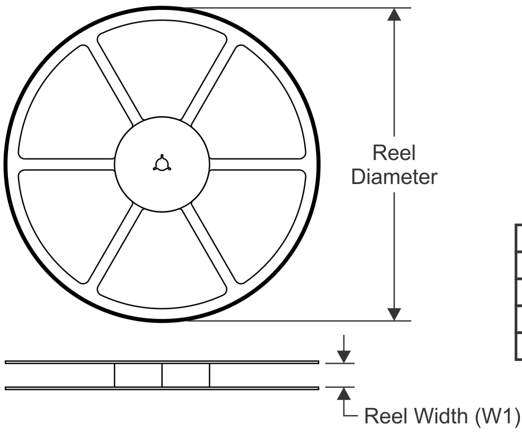
[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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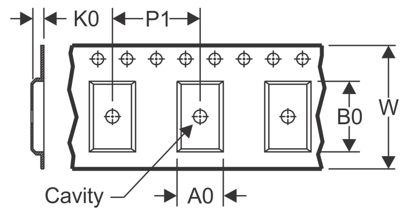
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

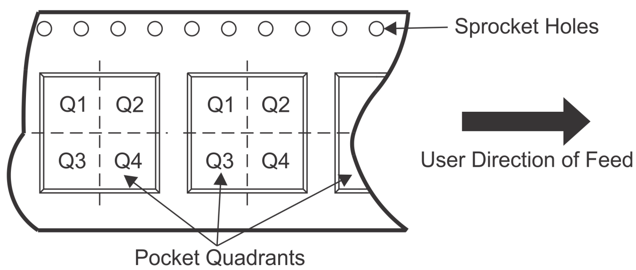


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

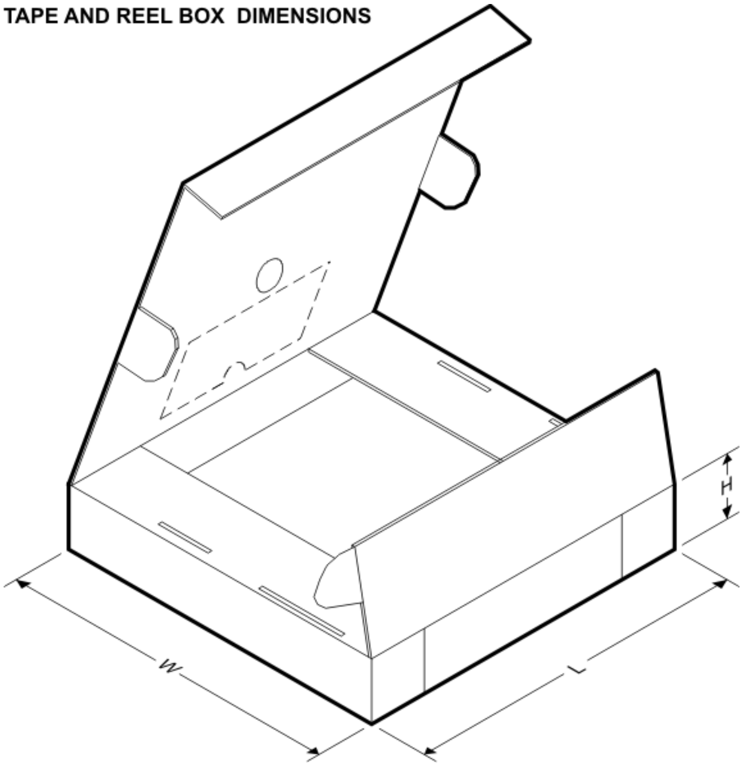
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM555CMM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM555CMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM555CMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM555CMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM555CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

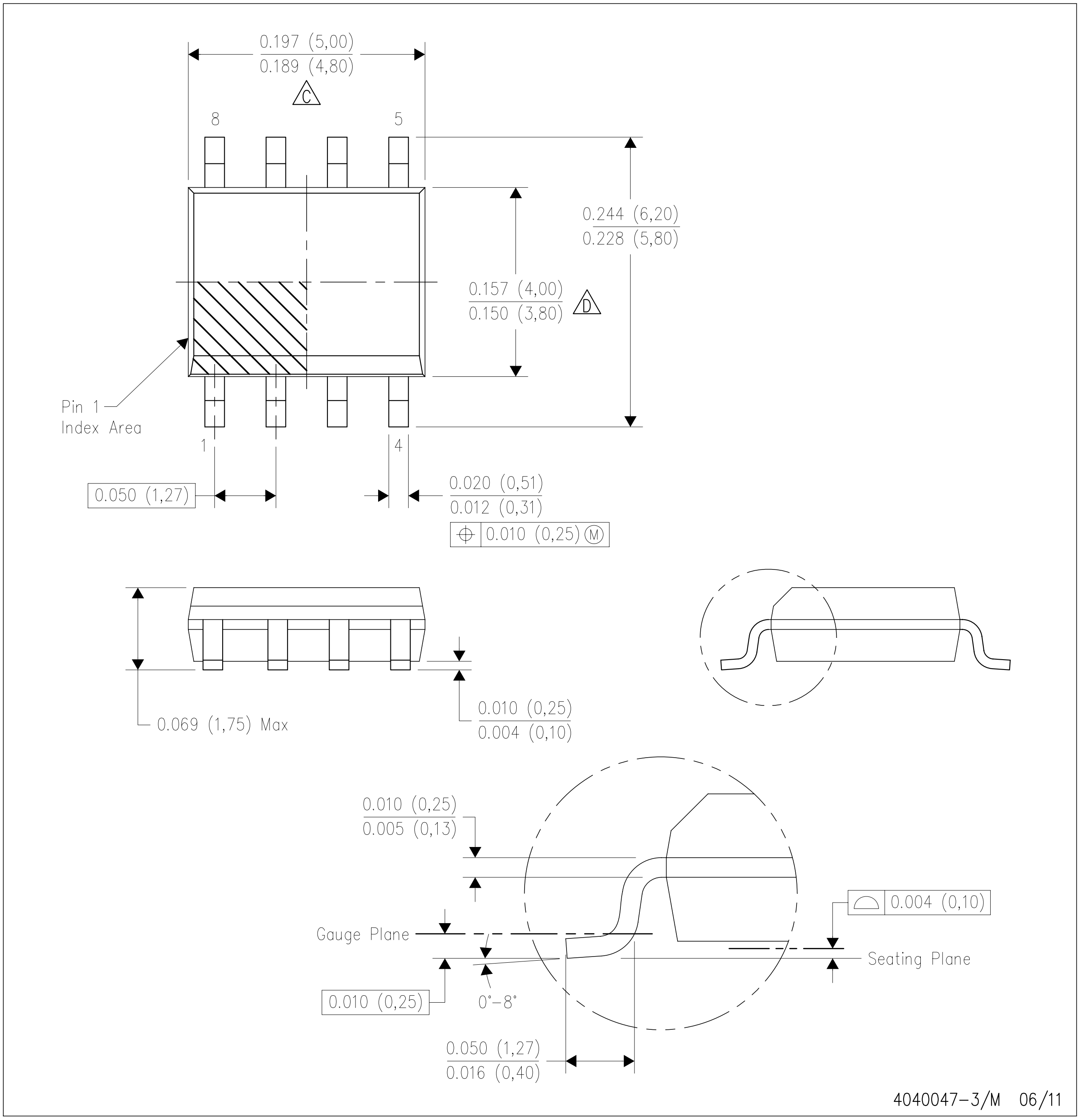
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

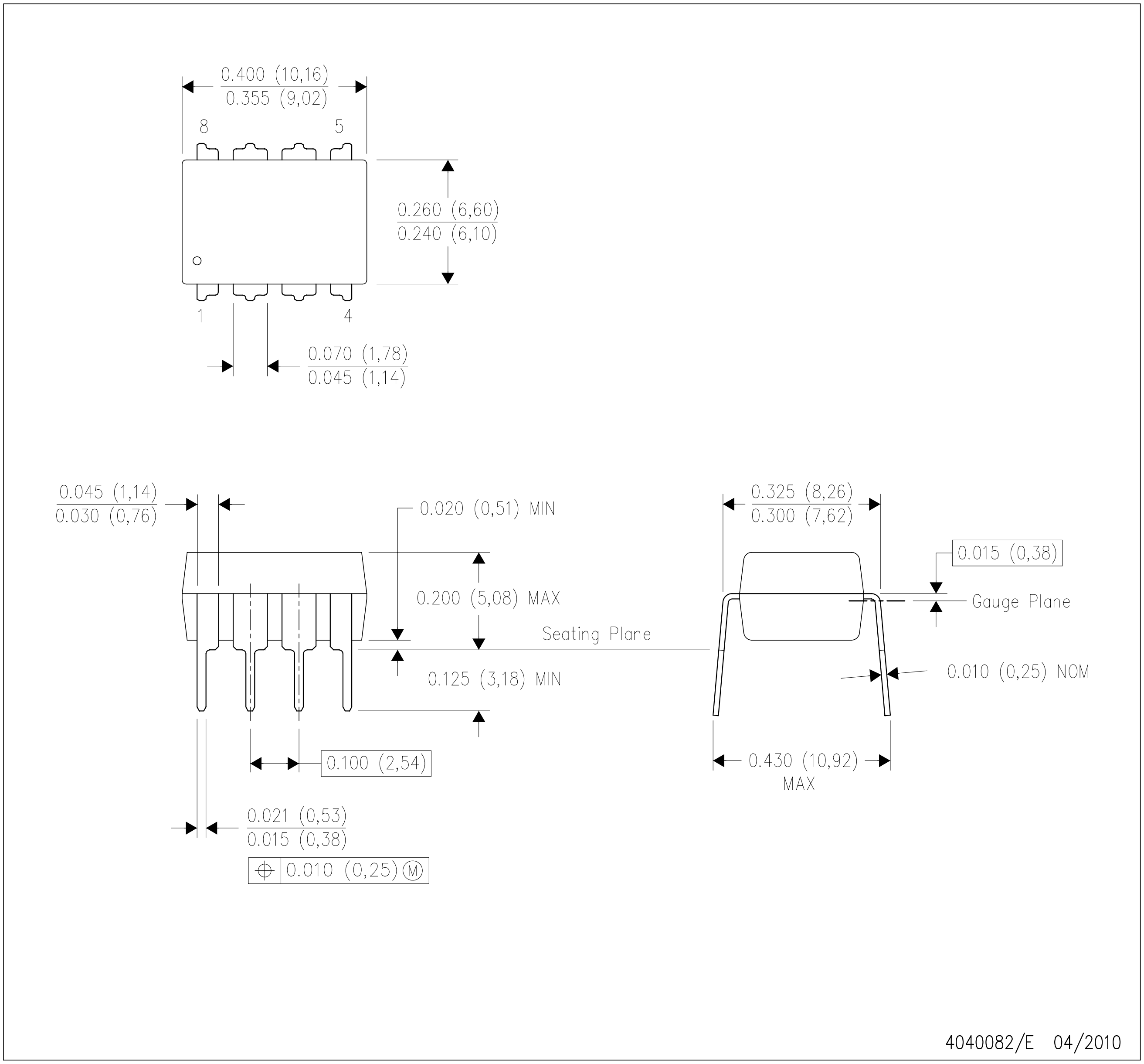
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM555CMM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM555CMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM555CMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM555CMX	SOIC	D	8	2500	367.0	367.0	35.0
LM555CMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



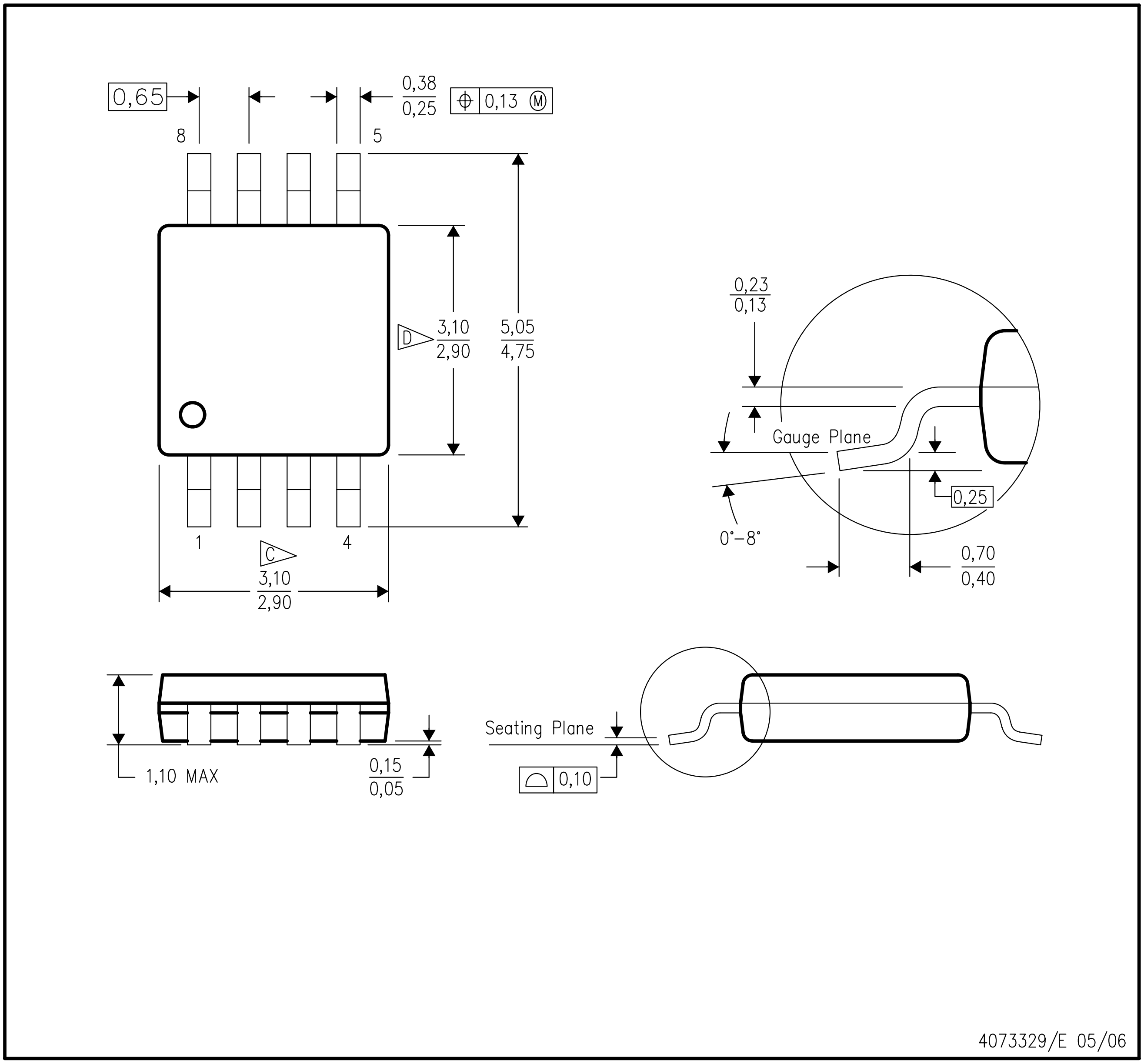
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

P (R-PDIP-T8) PLASTIC DUAL-IN-LINE PACKAGE



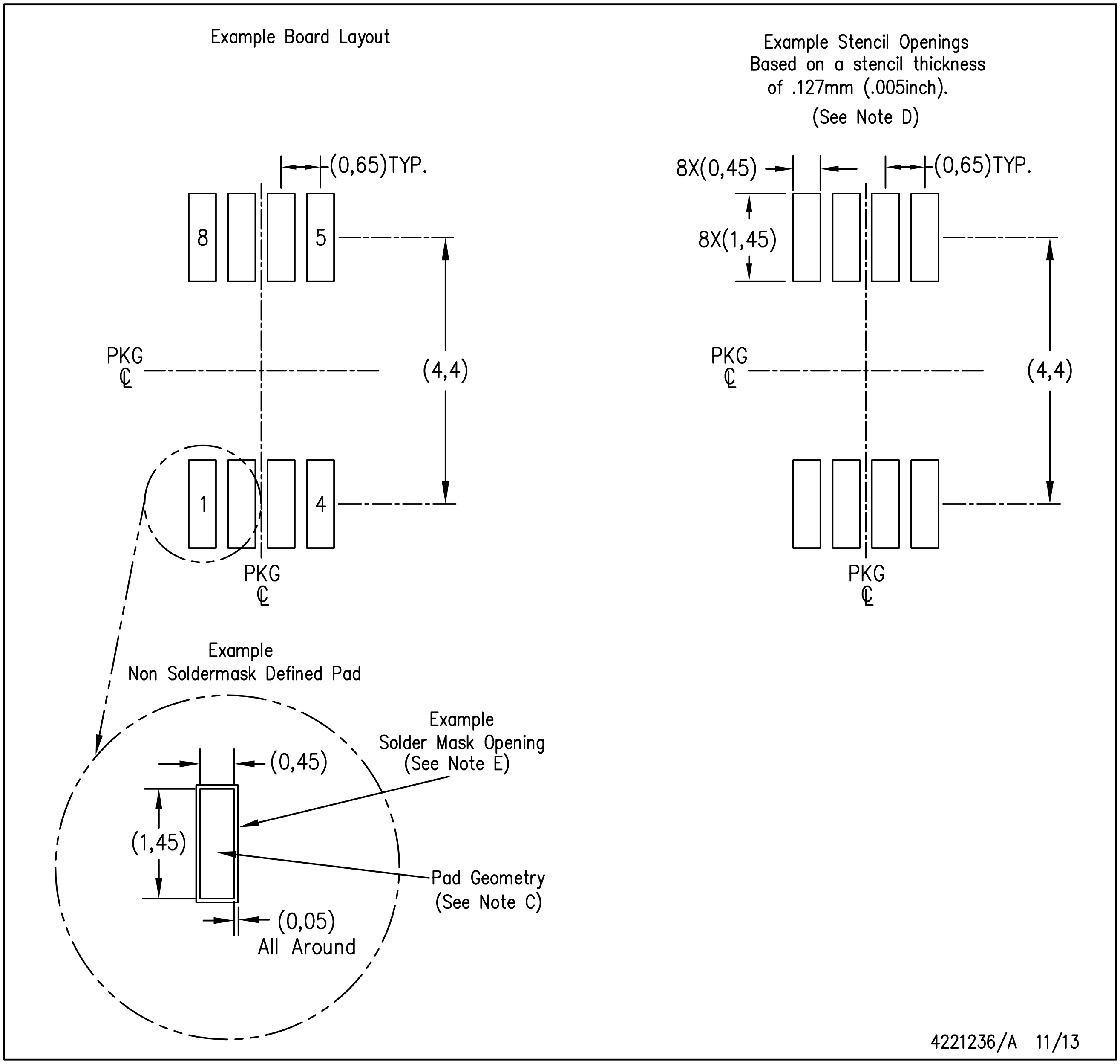
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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